

Attorney Docket No.: 0254-094-CIP4/CIP-MB

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Stacked Module Systems and Methods
Application No.: TBA
Filing Date: 04/20/2004
Inventor: Julian Partridge & James D. Wehrly, Jr.
Assignee: Staktek Group, L.P.
Examiner: TBA
Group: TBA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (five sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

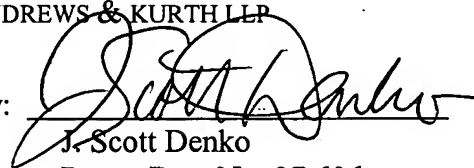
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Respectfully submitted,

ANDREWS & KURTH LLP

April 20, 2004
Date

By:



J. Scott Denko

Patent Reg. No. 37,606
111 Congress Ave., Suite 1700
Austin, Texas 78701
(512) 320-9200 Telephone
(512) 320-9292 Facsimile

Form PTO-1449 (Modified)
(Rev. 11/92)U.S. Dept. of Commerce
Patent and Trademark Office**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

(Use several sheets if necessary)

(37 CFR 1.98(b))

ATTY. DOCKET NO.

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254-094-CIP4/CIP-MB

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Julian Partridge & James D. Wehrly, Jr.

FILING DATE

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						Yes	No
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						Yes	No
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	Teresa Technologies, Inc. - Semiconductor Intellectual Property, Chip Scale Packaging - Website pages (3)

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